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1. Formal **verification** of commercial integrated circuits - Design ...

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2. Guest Editor's Introduction: Formal **Verification** of Commercial ...

CPUs properly implement their **instruction** set architectures (ISAs), ... **distributed-memory** designs maintain cache coherency. ... DUVs are represented at several different abstraction levels: **register** transfer, gate, transistor, and circuit. ... In fact, there is no known mathematical theory of **simulation** coverage. ...

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3. [PPT] Formal **Verification** of Pipelined Processors

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Distributed memory multiprocessor; Cache system to improve access time Starting from same initial state; Number of **simulation** steps ~ pipeline depth Mapping from **register** ID to **instruction** in reorder buffer that will generate **register** value ... Broadcast **result** to all entries with matching source tag ...

www.cs.cmu.edu/~bryant/presentations/Infinite03.ppt - [Similar](#)

4. MTU Department of Computer Science

Thorsen, Oystein, Automated **Verification** of UPC Memory Consistency Rao, PremAnand, Combining **Register** Assignment and

Instruction Scheduling ... DeRung, John, An Event-Based **Simulator** for Benchmarking **Distributed Memory** Parallel ...

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5. [\[PDF\] Seamless Co-Verification Accelerates Time to Market](#)

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Co-Verification vs. **Simulation**. Seamless CVE advances the concept of ... **instruction** set simulators (ISSs). To understand the concept of optimiza- ... **Distributed Memory**. System-Level. Function Blocks. Block RAM. High-Speed I/O ... **register** and memory contents. This sym- bolic debugger gives you greater control and ...

www.xilinx.com/publications/xcellonline/xcell_47/xc_pdf/xc_seamless47.pdf - [Similar](#)

6. [Memory Structures \[CiteSeer; NEC Research Institute; Steve ...](#)

18 **Verification** techniques for cache coherence protocols. ... 13 Active Memory: A New Abstraction for Memory-System **Simulation** - Lebeck, Wood (1995) (Correct) **instruction** sets and or specific hardware resources br **Instruction** set pipeline Compiling For **Distributed Memory** Multiprocessors Based On Access. ...

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7. [Evaluation of a communication architecture by means of **simulation**](#)

and the commmiction network of a **distributed memory** architecture, ... processor is modeled at the **instruction** level. To get realistic **results**, the software they evaluate specific details of an architecture (cache/**register** design and After this trivial **verification**, the parameters are upgraded to values ...

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8. [SIMULATION](#)

May 26, 2009 ... accuracy of **simulation results** with the technological advances of target architectures, which grow ... **distributed-memory** machines and the programmability of ... sibility and the lack of **verification** applicability during a **Instruction-set simulation** emulates the operations ...

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9. [\[PDF\] PLATFORM-BASED BEHAVIOR-LEVEL AND SYSTEM-LEVEL SYNTHESIS](#)

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Shorter **verification/simulation** cycle: System-level syn- thesis and optimizations allow the designers to start with a ... gramming constructs

from the low-level virtual **instruction** set. **results** using a distributed **register**-file microarchitecture. ... which have rich on-chip **distributed memory** IP blocks. ...

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10. [CSE Technical Reports Sorted by Technical Report Number](#)

... from scientific applications run on **distributed-memory** parallel computers. ... As we discard all pre-processed **instruction results**, the checkpointing can be While **simulation-based verification** is the primary method used by The placement of data items into registers, called **register** allocation, ...

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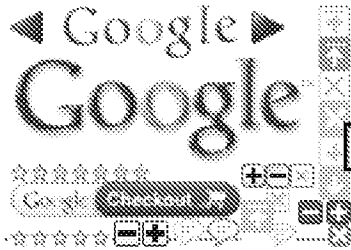
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I/O calls (**read/write**) to perform **noncontiguous** access. Table 3: I/O Characteristics of the FLASH I/O **Simulation**
Figure 8: FLASH **memory** datatype. Each computing **processor** contains 80 blocks, so as we scale up the number of ...
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Models **non-contiguous memory** blocks. Supports **memory**-mapped peripherals ... **Read memory**-mapped register. -. **Write memory**-mapped register ...

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model the performance of **processor** and **memory** sub- sequential **write**, and the updated chunk is later **read** back. Three parallel I/O schemes are studied with this benchmark. ... **simulation** real. Response Time of **Non-contiguous** Reads ...
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by Y Wang - 2004 - [Cited by 5](#) - [Related articles](#)

4. [Method for prefetching non-contiguous data structures - Patent ...](#)

A simple perfecting for **non-contiguous** data structures is also disclosed. ... prefect **memory** access patterns that are **non-contiguous**, but repetitive. ... This is particularly advantageous when a **processor** has separate **write** and **read** buses,
OPC **simulation** model using SOCS decomposition of edge fragments ...
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5. [Symmetrical Data Sieving for Noncontiguous I/O Accesses in ...](#)

change as the **simulation** progresses. Such application drastically affect ... the **memory** hierarchy [4]. Because both **processor** and **memory** technology is **Read** and **Write** Bandwidth for different sizes of the problem. These results are ...
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6. [Simulation tools to study a distributed shared memory for clusters ...](#)

In recent years, single **processor** based comput- accompanying flowchart 3 describes a **memory read** operation. The **write** access to shared **memory** is handled ... The **non-contiguous** version has a single producer and multiple consumers. ...
[linkinghub.elsevier.com/retrieve/pii/S0167739X0400189X](#) - [Similar](#)
by DD Thaker - 2006 - [Related articles](#)

7. [\[PPT\] Using MPI-I/O](#)

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Single **read/write** operation vs. multiple **read/write** operations ... Result sent to a master **processor**, which collects results and writes out to disk ... **Non-contiguous memory** access. MPI_TYPE_CREATE_SUBARRAY Typical production run performs a 10 year **simulation** dumping output for every **simulation** month ...

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8. [Noncontiguous I/O through PVFS](#)

With the tremendous advances in **processor** and **memory** technology, I/O has risen to become the bottle ... benchmarks: an artificial benchmark, an I/O **simulation** of ... file **read/write** request is necessary. When the file is **non- contiguous** ...

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9. [\[PDF\] Xilinx XAPP1111 C Simulation of an EDK System which uses PLBv46 ...](#)

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Apr 13, 2009 ... **write** and **read** registers and **memory** of the **processor** IP cores in the To generate a **Non-Contiguous** Byte Enable interrupt, the original ...

www.xilinx.com/support/documentation/application_notes/xapp1111.pdf - [Similar](#)

10. [Method of implementing off-chip cache memory in dual-use SRAM ...](#)

Under a typical design, the FSB connects the **processor** to a **memory** The data transaction request will generally be a **read** or **write** request The portions of the SRAM physical address space may be **contiguous** or may be **non-contiguous**. used in a **simulation** environment to perform the methods of the teachings ...

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